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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-004143
(43)Date of publication of application : 06.01.1998

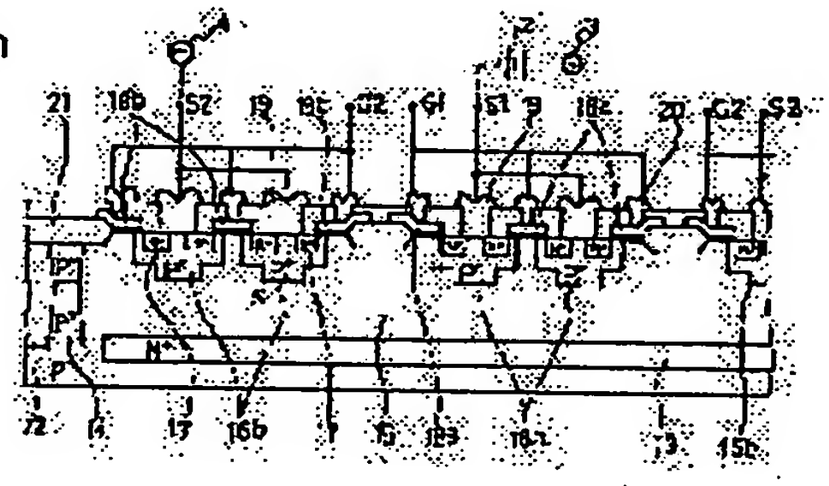
(51)Int.Cl. H01L 21/8234
H01L 27/088
H01L 29/78

(21)Application number : 08-154246
(22)Date of filing : 14.06.1996

(71)Applicant : SANYO ELECTRIC CO LTD
(72)Inventor : OTAKE SEIJI

(54) SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the loss of a circuit by integrating two MOSFET elements inside a common island region and making a common drain.
SOLUTION: An epitaxial layer 12 formed on a substrate is isolated to form an island region 15, and on the surface of the island region 15 P-type diffusion regions 16a, 16b, source regions 17, and gate electrodes 18a, 18b are formed. First and second MOSFET elements are formed by electrode wiring. By making the island region 15 a common drain, drain connection of the both is realized.



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[Date of request for examination]

[Date of sending the examiner's decision of rejection]

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[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報(A)　(11)特許出願公開番号

特開平10－4143

(43)公開日　平成10年(1998)1月6日

(51)Int.Cl.⁶		識別記号	庁内整理番号	FI		技術表示箇所
H01L	21/8234			H01L	27/08	102B
	27/088				29/78	301D
	29/78					

審査請求　未請求　請求項の数3　OL　（全 4 頁）

(21)出願番号　特願平8－154246

(22)出願日　平成8年(1996)6月14日

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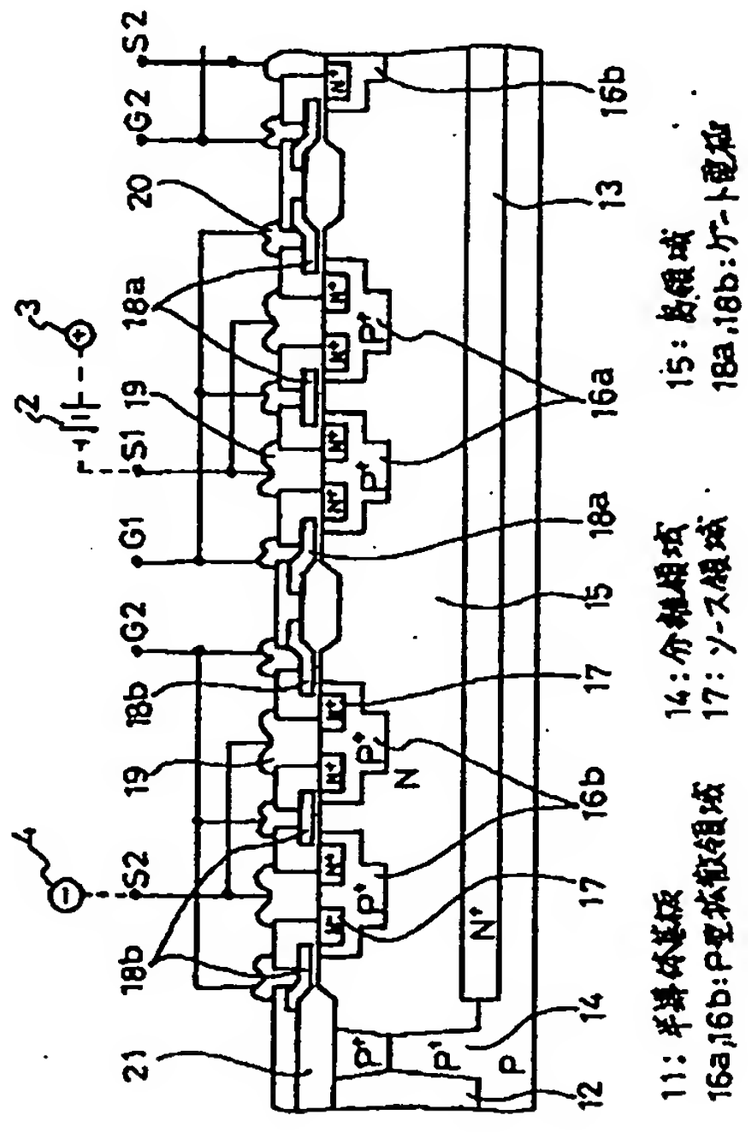
(54)【発明の名称】　半導体集積回路

(57)【要約】

【課題】　２つのＭＯＳＦＥＴ素子を共通の島領域内に集積化して共通ドレインとすることによりドレイン抵抗を減じて回路損失の低減を図る。

【解決手段】　基板１１上に形成したエピタキシャル層１２を分離して島領域１５を形成し、島領域１５表面にＰ型の拡散領域１６ａ、１６ｂ、ソース領域１７、そしてゲート電極１８ａ、１８ｂを形成する。電極配線により第１と第２のＭＯＳＦＥＴ素子５、６を形成する。島領域１５を共通ドレインとすることにより両者のドレイン接続を実現する。



【特許請求の範囲】
【請求項１】　ドレインが互いに接続され、２次電池に直列に接続されると共に前記２次電池の充放電を制御する少なくとも２つのＤＳＡ（Double Diffused Self Alignment）型ＭＯＳトランジスタを具備する半導体装置であって、
一導電型の半導体基板の上に形成した逆導電型のエピタキシャル層を一導電型の分離領域により接合分離して島領域とし、
１つの前記島領域に、チャンネルとなる一導電型の拡散領域と逆導電型のソース領域及びゲート電極を形成して前記２つのＤＳＡ型ＭＯＳトランジスタを形成し、
前記２つのトランジスタの第１のゲートと第２のゲートの間に逆導電型の共通ドレイン領域を設けて、前記２つのトランジスタのドレインを互いに接続したことを特徴とする半導体集積回路。
【請求項２】　前記ＤＳＡ型ＭＯＳトランジスタが縦型のＤＳＡ型ＭＯＳＦＥＴであることを特徴とする請求項１記載の半導体集積回路。
【請求項３】　前記ＤＳＡ型ＭＯＳトランジスタが横型のＤＳＡ型ＭＯＳＦＥＴであることを特徴とする請求項１記載の半導体集積回路。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、リチウムイオン、ニッケル水素などの充電可能な２次電池の充電回路に使われるＤＳＡ型のＭＯＳＦＥＴ素子を集積化した半導体集積回路に関する。
【０００２】
【従来の技術】リチウムイオン、ニッケル水素などの充電可能な２次電池は、ニッケルカドミウム電池に比べて容量を大きくできる反面、過電圧、過電流、過充電により電池性能が大幅に低下する欠点を合わせ持つ。そのため２次電池の端子間電圧を常時監視し、前記過充電等から前記２次電池を保護するための制御回路を具備する必要がある。そして、制御用のＩＣと共に電圧駆動が可能なＤＳＡ（Double Diffused Self Alignment）型のパワーＭＯＳＦＥＴ素子を電池パック内に内蔵し、前記パワーＭＯＳＦＥＴで２次電池の充放電流を制御することで電子機器の低消費電力化を図ることが多い。
【０００３】電池パック内に内蔵される回路の一例を図３に示す。図中、１は制御用のＩＣ、２はリチウムイオン電池、３及び４は電池パック外部に導出される正極端子及び負極端子、５及び６は第１及び第２のＭＯＳＦＥＴ素子である。第１と第２のＭＯＳＦＥＴ素子５、６はドレインを共通接続しており、各々のゲートは制御用ＩＣ１の制御端子に接続されている。そして、前記過電圧、過電流、過充電時には制御ＩＣからの制御信号を受けて第１と第２のＭＯＳＦＥＴ素子５、６の両方又はどちらか一方がＯＦＦする事により、リチウムイオン電池２に流れる電流をカットして電池を保護するような動作を行う。
【０００４】
【発明が解決しようとする課題】図３の回路において、リチウムイオン電池２が放電動作を行う時、第１と第２のＭＯＳＦＥＴ素子５、６に図示矢印ｉのような動作電流を流すことになる。この時の抵抗成分Ｒは、ＭＯＳＦＥＴ素子５、６のＯＮ抵抗や配線抵抗等により決まるものであるが、この値が大きいと前記動作電流により発熱し、該発熱は動作電流の損失となるので、２次電池の電池寿命を低下させることになる。そのため、抵抗成分Ｒを低下させることが電池寿命を延ばす鍵になっていた。
【０００５】
【課題を解決するための手段】本発明はかかる従来の課題に鑑みなされたもので、第１と第２のＭＯＳＦＥＴ素子を１チップ化したものであり、且つ、第１と第２のＭＯＳＦＥＴ素子を共通の島領域内部に形成し、島領域を共通ドレインとして互いのドレインを接続し、アルミ電極を省略することにより、抵抗成分を大幅に低減して電池寿命を改善できる半導体装置を提供するものである。
【０００６】
【発明の実施の形態】以下に本発明を図面を参照しながら詳細に説明する。図１は本発明による半導体集積回路を示す断面図、図２はその平面図である。まずは縦型のＤＳＡ型ＭＯＳＦＥＴ（Ｖ－ＤＭＯＳ）を図示してある。なお、図５中の符号と一致する箇所には同じ符号を付している。
【０００７】同図において、１１はＰ型の単結晶シリコン半導体基板、１２は基板１１の上に気相成長して形成したＮ－型のエピタキシャル層、１３は基板１１とエピタキシャル層１２との間に埋め込んで形成したＮ＋型の埋め込み層、１４はエピタキシャル層１２を貫通してエピタキシャル層１２を複数の島領域１５に形成するＰ＋型の分離領域、１６ａ、１６ｂは島領域１５の表面に形成した複数のＰ型拡散領域、１７はＰ型拡散領域１６の表面に形成したＮ＋型のソース領域、１８ａ、１８ｂはソース領域１７近傍の上に形成したポリシリコンゲート電極、１９はソース領域１７とＰ型拡散領域１６の両方にオーミックコンタクトするソース電極、２０はアルミゲート電極、２１はＬＯＣＯＳ酸化膜である。
【０００８】ゲート電極１８ａとＰ型拡散領域１８ａが第１のＭＯＳＦＥＴ素子５を構成し、同じくゲート電極１８ｂとＰ型拡散領域１８ｂが第２のＭＯＳＦＥＴ素子６を構成する。具体的には同じ島領域１５内に単位ＭＯＳセルが多数個作られ、これらがアルミ電極により並列接続されて大きな２つのＭＯＳＦＥＴ素子５、６を構成する。隣接するＰ型拡散領域１６ａ、１６ｂの間にはＬＯＣＯＳ酸化膜が形成される。
【０００９】第１のＭＯＳＦＥＴ素子５のゲート電極１８ａはＩＣ表面を引き回されて同じＩＣ内部の別の箇所

に形成した制御回路の制御端子Ｇ１に接続される（図５参照）。同じく第１のＭＯＳＦＥＴ素子６のソース電極１９はＩＣ表面の外部接続パッドＳ１に接続され、電源パックとしては２次電池２の負極端子に接続される。２次電池２の負極端子は電源パックの正極端子３となる。

【００１０】第２のＭＯＳＦＥＴ素子６のゲート電極１８ｂはＩＣ表面を引き回されて同じＩＣ内部の別の箇所に形成した制御回路の制御端子Ｇ２に接続される。同じく第２のＭＯＳＦＥＴ素子６のソース電極１９はＩＣ表面の外部接続パッドＳ２に接続され、電源パックの正極端子４となる。図２を参照して、ゲート電極１８ａとゲート電極１８ｂとは櫛歯状に形成され、互いにかみ合うようにし配置することで、第１のＭＯＳＦＥＴＴ素子５を構成するセルと第２のＭＯＳＦＥＴ素子６を構成するセルとが互い違いに隣接するように配置している。

【００１１】第１のＭＯＳＦＥＴ素子５と、第２のＭＯＳＦＥＴ素子６は、一つの島領域１５を共通ドレインとして一つの島領域１５内に形成される。図４の回路図に従えば、両者のドレインは電気的に接続されていればよく、他に接続箇所がないので、島領域１５表面にドレイン電極を導出する必要はない。本発明によれば、第１と第２のＭＯＳＦＥＴ素子５、６を集積化したことにより電流パスが短くなるのでドレイン接続に要する電気抵抗を減じることができる。さらに第１と第２のＭＯＳＦＥＴ素子５、６を共通の島領域１５に形成したことにより、島領域１５を共通ドレインにできるので、ドレイン接続のアルミ電極を不要として電流パスを短くでき、例えば両者を別々の島領域１５に形成して電極接続する場合に比べてアルミ電極の引き回しが無い分、ドレイン接続に要する電気抵抗を大幅に減じることができる。

【００１２】図３と図４はＭＯＳＦＥＴ素子として横型のＤＳＡ型ＭＯＳＦＥＴ（Ｌ－ＤＭＯＳ）を形成した場合の実施の形態を示す断面図と平面図である。同じ箇所には同じ符号を伏して説明を省略する。図１の縦型と異なりドレイン電流を基板１１と水平方向に流すので、島領域１５表面にドレイン領域２２を具備する。Ｐ型拡散領域１６ａ、ドレイン領域２２、Ｐ型拡散領域１６ｂ、ドレイン領域２２、Ｐ型拡散領域１６ａ、と言うように交互に配置する。ドレイン領域２２は電流パスの抵抗値を下げる働きをする。先の形態と同様にドレイン電極は必要ない。本実施の形態においても、島領域１５を共通ドレインとすることにより電流パスを最短にできるので、ドレイン接続に要する電気抵抗を大幅に減じることができる。

【００１３】

【発明の効果】以上に説明したとおり、本発明によれば、第１と第２のＭＯＳＦＥＴ素子５、６を共通の島領域１５内に配置し、島領域１５を共通ドレインとすることにより両者のドレインを接続したので、ドレイン接続に伴う電流経路の抵抗成分を大幅に減じることができる。従って図５の抵抗成分Ｒを大幅に減じることができるので、動作に伴う発熱を減じ損失を低減できるので２次電池の電池寿命を延長できる利点を有する。さらにドレイン電極を引き回す必要が無くなるので、アルミ配線を簡素化して面積の縮小を図ることができる。

【図面の簡単な説明】

【図１】本発明を説明するための断面図である。

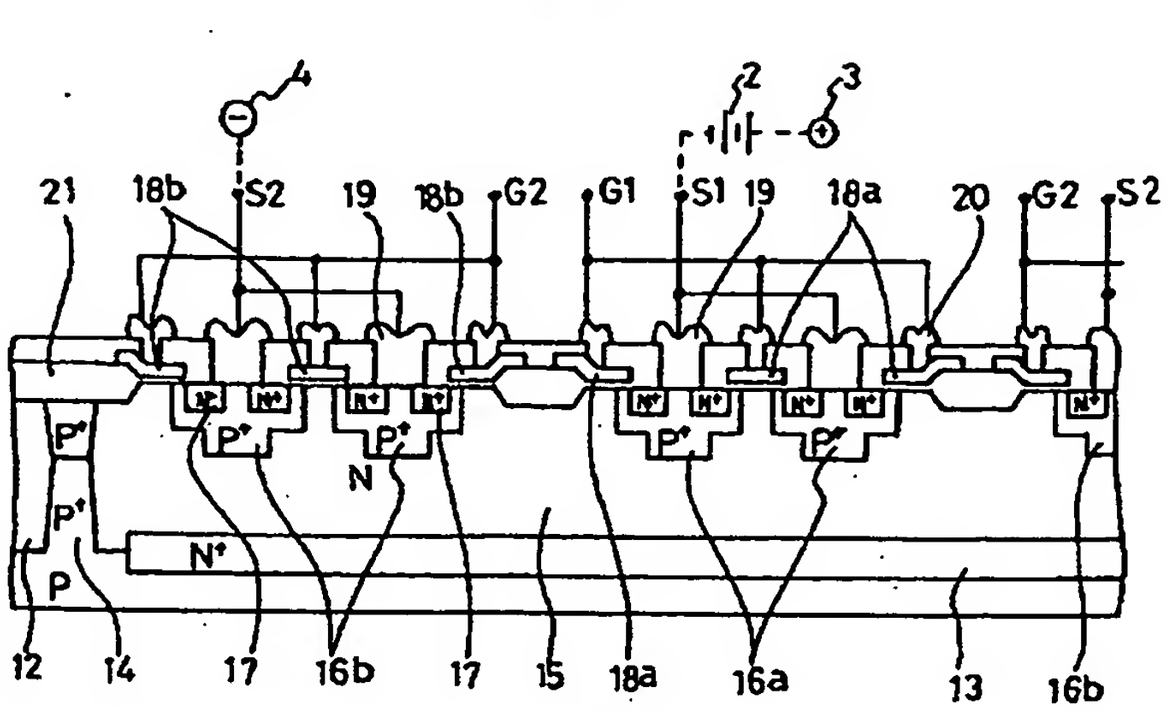
【図２】本発明を説明するための平面図である。

【図３】本発明の第２の実施の形態を説明するための断面図である。

【図４】本発明の第２の実施の形態を説明するための平面図である。

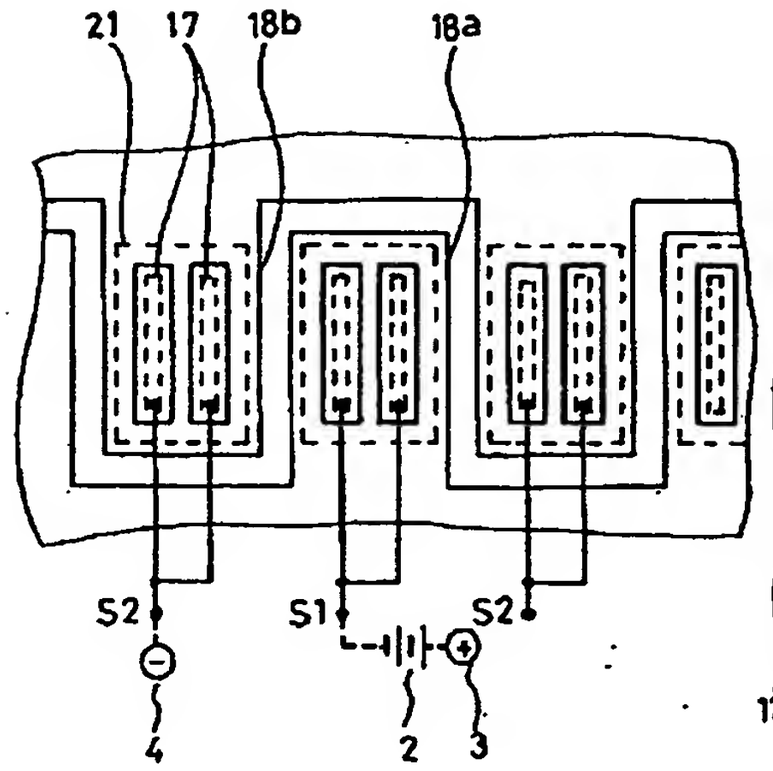
【図５】従来例を説明するための回路図である。

【図１】



11：半導体基板　　14：分離領域　　15：島領域
16a,16b：P型拡散領域　　17：ソース領域　　18a,18b：ゲート電極

【図2】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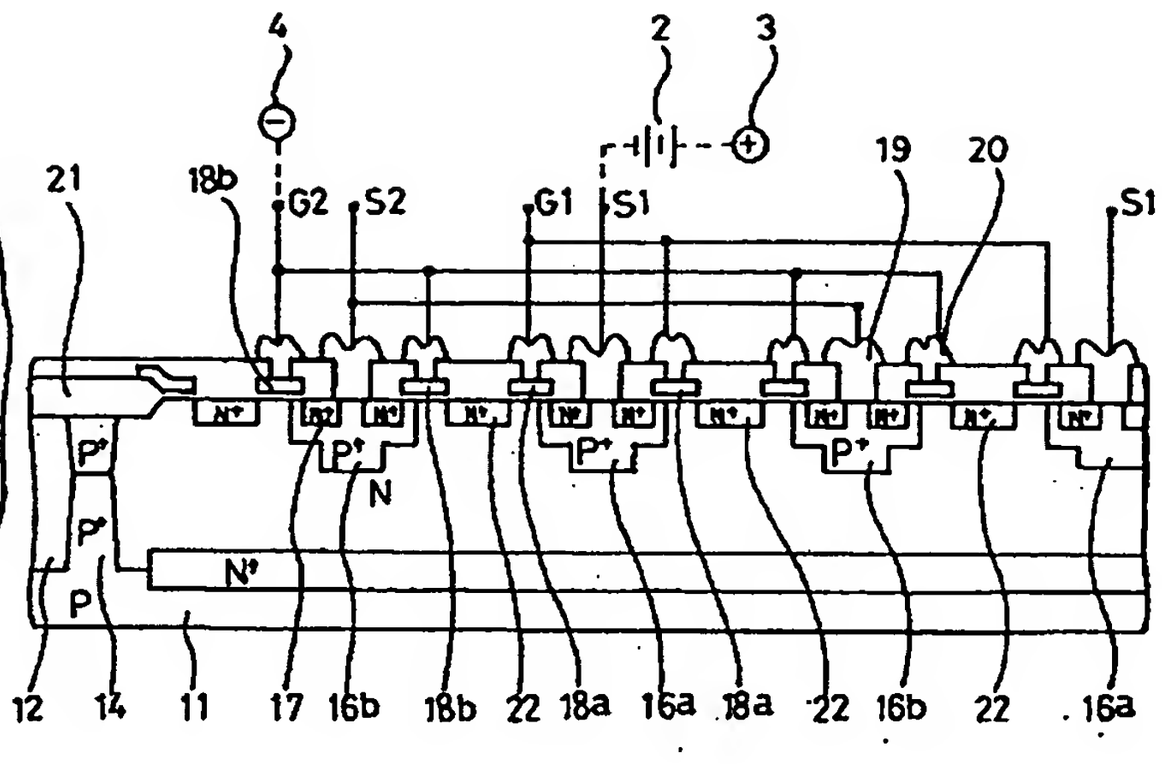
18a
S2
S1
S2
4
2
3

【図3】


4
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21
18b
G2
S2
G1
S1
19
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N+
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12
14
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16a
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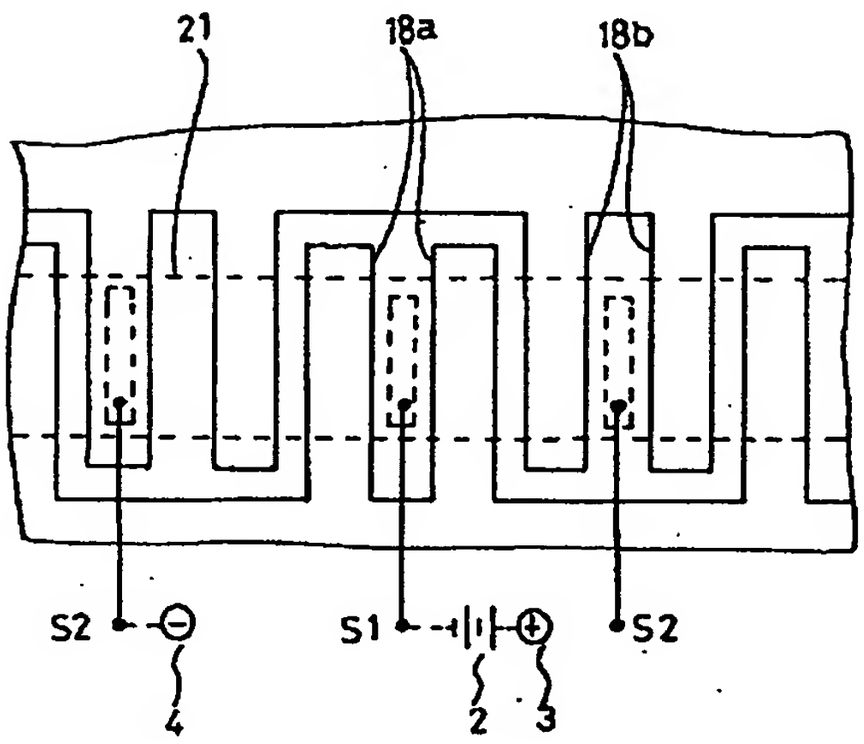
16b
22
16a

【図4】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18a
18b
S2
S1
S2
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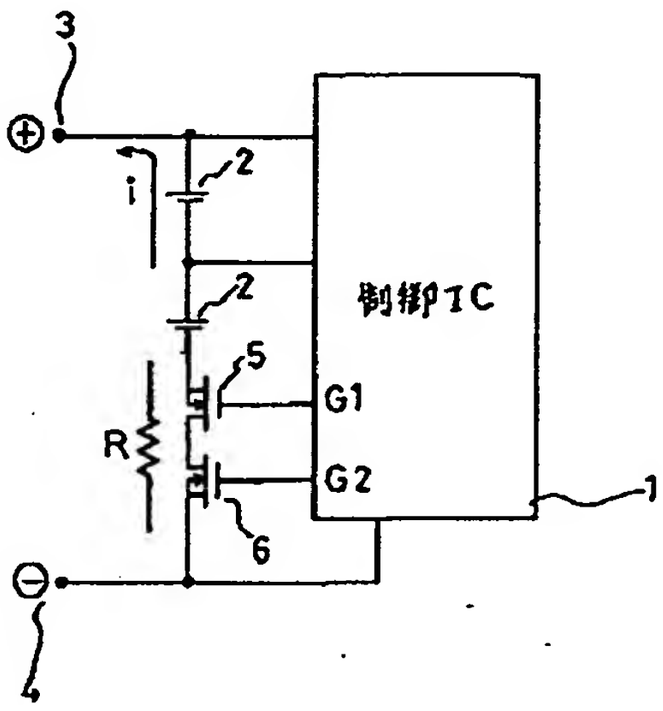
【図5】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The 5th International Symposium on
Power Semiconductor Devices and ICs

ISPSD '93

May 18-20, 1993 Monterey, California, USA

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IEEE Catalog Number: 93CH3314-2

1200V High-Side Lateral MOSFET in Junction-Isolated Power IC Technology Using Two Field-Reduction Layers

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Abstract

A lateral n-channel MOSFET structure in Junction-Isolated Power IC Technology using a P type field-reduction region over a N type field-reduction region for high-side and low-side switching applications is described. The concept of using two field-reduction layers have been verified by two-dimensional device simulations and by fabricating devices with breakdown voltage in excess of 1200V.

Introduction

In Power ICs in Junction-Isolated Technology, the control circuit consisting of low-voltage CMOS and bipolar devices can be easily integrated with a lateral power device when the substrate is at ground potential. For high-voltage lateral devices in Power ICs, a surface field-reduction region is widely used [1]. In lateral n-channel MOSFET structure with a single field-reduction layer (Fig. 1), the charge in the field-reduction region (N-) is such that it is completely depleted when the drain is at the line voltage and the source/body and substrate are at ground potential. This is useful for low-side switching applications.

There are many applications for power semiconductor switching devices which put the semiconductor device on the high-side. In those circuit applications, the semiconductor switch is connected between the high voltage line potential and the load. Consequently, both the source and drain electrodes of the power semiconductor switch will be placed at the high line potential while the substrate is at ground potential. If the conventional lateral MOSFET structure with a single field-reduction layer is used, the field-reduction layer would be completely depleted in this condition leading to PNP punch-through breakdown from the body region to the substrate. Consequently, Dielectric-Isolation Technology or discrete power MOSFETs with separate off-chip controls are used in high-side switching applications. The discrete device solution is costly in most applications. Dielectric-Isolation Technology has problem of heat-dissipation and is also costly.

In this paper, simulation and experimental results of a lateral n-channel MOSFET structure [2] which uses two-field reduction layers is described. The charge in the N and P field-reduction layers and the field-reduction region length were varied in devices fabricated to look at influence of these parameters on breakdown voltage and on-state characteristics.

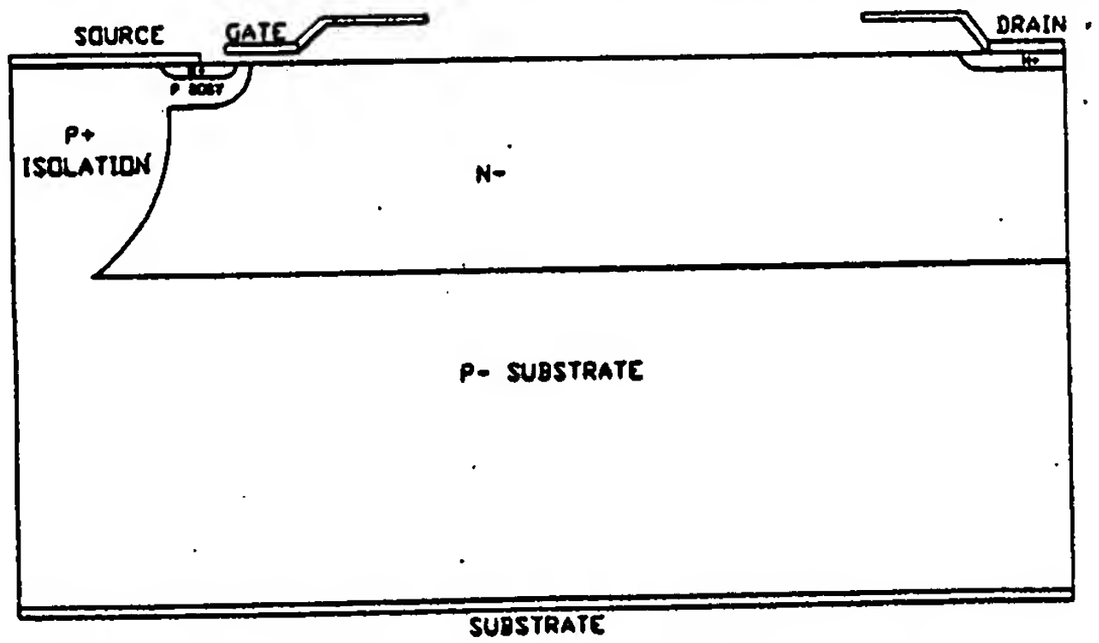

Fig. 1. Lateral n-channel MOSFET structure using a single field-reduction region

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5th International Symposium on Power Semiconductor Devices and ICs

Device Concept

The new device structure is shown in Fig 2 for high-side configuration. Fig 3 shows the device structure in this technology for low-side configuration. The device uses a P type field-reduction layer over a N type field-reduction layer. The charge in the top (P-) field-reduction layer is chosen to be approximately $1x10^{12}$ cm^{-2} and the charge in the N- field-reduction layer is chosen to be from $1.5x10^{12}$ cm^{-2} to $2x10^{12}$ cm^{-2}. This enables the use of the device as a high-side switch in Power ICs. In a high-side switching configuration, the drain is connected to the high line voltage.

When the high-side device is in the off-state, the body/source will be close to the substrate potential and should support the line voltage relative to the drain region. The charge in the field-reduction layers are chosen such that both the P- and N- field-reduction layers are completely depleted in this condition.

The N- field-reduction layer is depleted from both the top field-reduction layer and the bottom P- substrate. T determines the charge in the P- field-reduction la (approximately $1x10^{12}$ cm^{-2}) and also imposes an upper li on the charge in the N- field-reduction layer (< $2x10^{12}$ cm

The two-layered field-reduction structure also permits b the body/source region and the drain region to be pla close to the line voltage relative to the grounded substr This is the situation when the device is in the on-state. In case, the N- field-reduction layer depletes only from bottom P- substrate. The charge in the N- region should high enough (> $1x10^{12}$ cm^{-2}) to prevent full deplet (preventing punch-through from the body region to substrate) as well as providing sufficient undepleted charg form a low resistance conduction path from the source to drain through the N- lateral field-reduction region.

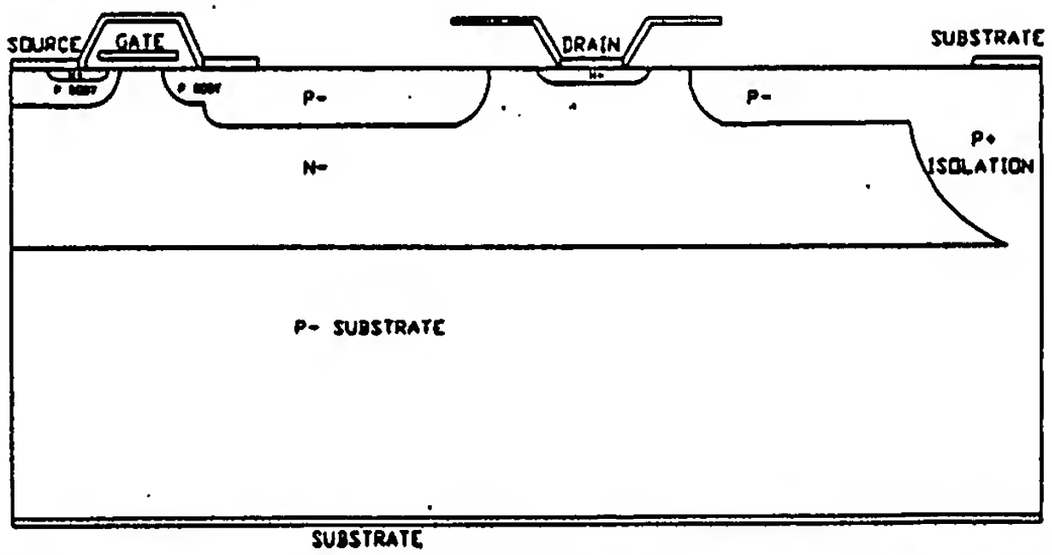

Fig. 2. Lateral n-channel MOSFET structure using two field-reduction layers for high-side switching applications

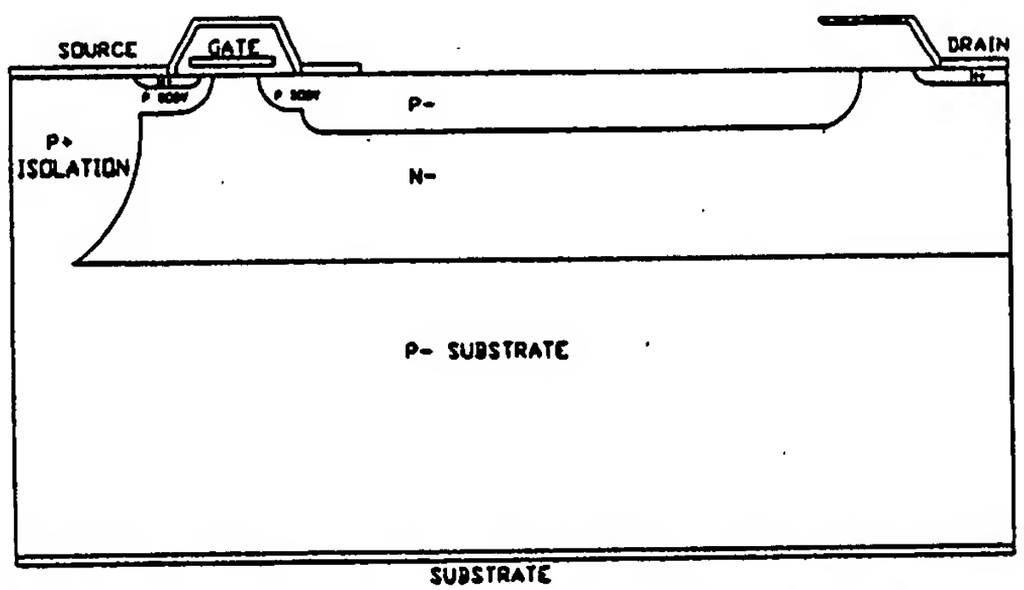

Fig. 3. Lateral n-channel MOSFET structure using two field-reduction layers for low-side switching configuration

Device Simulation

Two-dimensional device simulations using PISCES-2B was used to get an insight into the device physics. The parameters used for device simulations are indicated in Table 1. The doping profile of the P- field-reduction region was obtained from SUPREM-3 process simulations.

A P- implant dose of 4×10^{12} cm^{-2} was used in the process simulation. The potential contours obtained from PISCES simulations are shown in Fig 4 and Fig 5 for the device off-state and on-state respectively. Fig 6 and Fig 7 shows the variation of potential through a vertical cross-section of the device at the center of the P- field-reduction region in the off-state and on-state respectively.

Table 1. Parameters used for PISCES-2B two-dimensional device simulations

PARAMETER	VALUE
P- substrate doping (uniform)	1.2×10^{14} cm^{-3}
N- epi doping (uniform)	1.2×10^{15} cm^{-3}
N- epi thickness	20 μm
P- field-reduction region length	120 μm
Spacing between P- field-reduction layer & N+ drain diffusion windows	15 μm
Polysilicon gate length of DMOSFET	8 μm
Gate oxide thickness	1000 Å
Minority carrier lifetime	1 μs

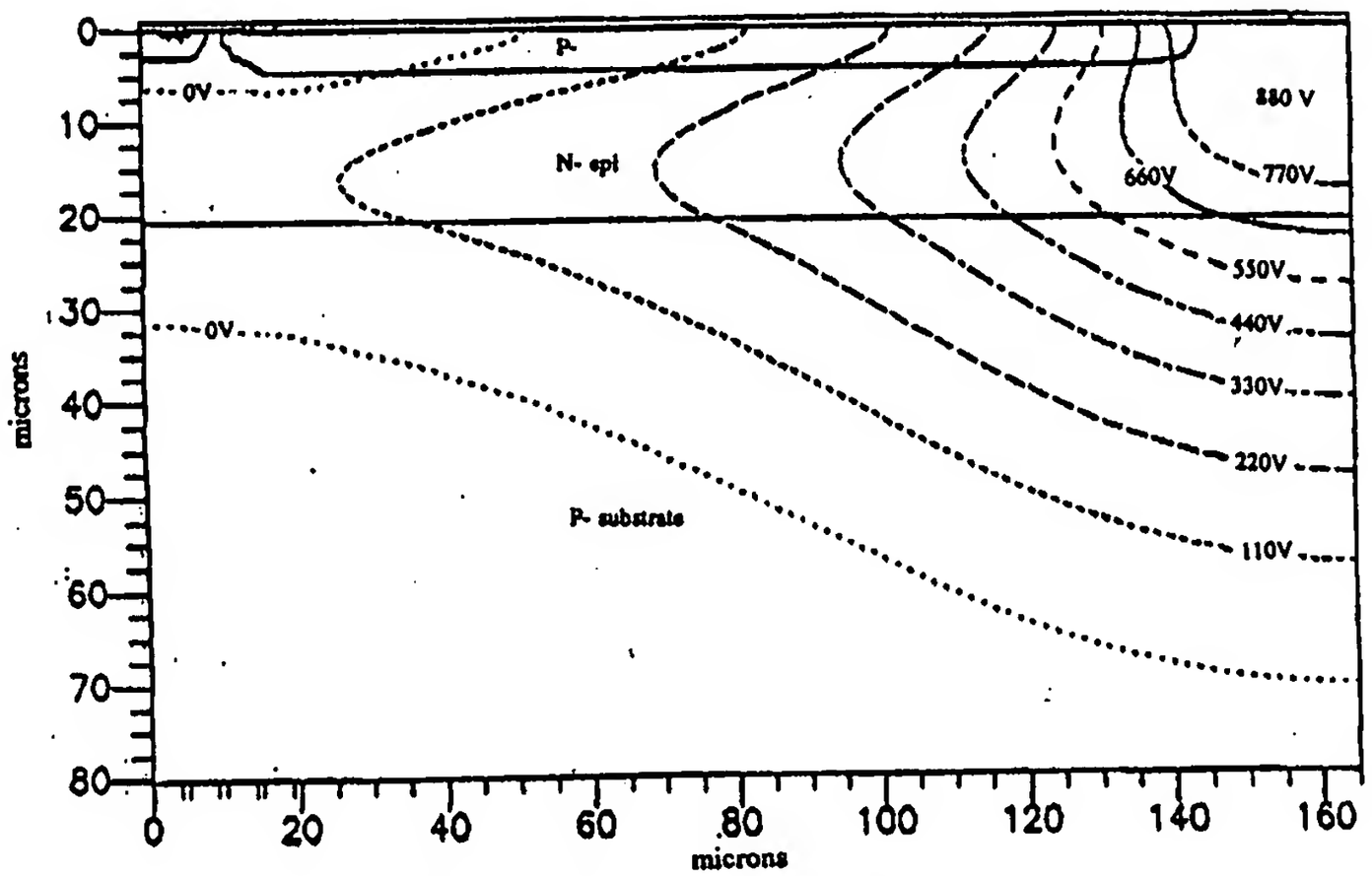

Fig. 4. Potential contours in the "two field-reduction layer" structure in the off-state (Drain at a high potential relative to the grounded source and substrate) from PISCES simulations

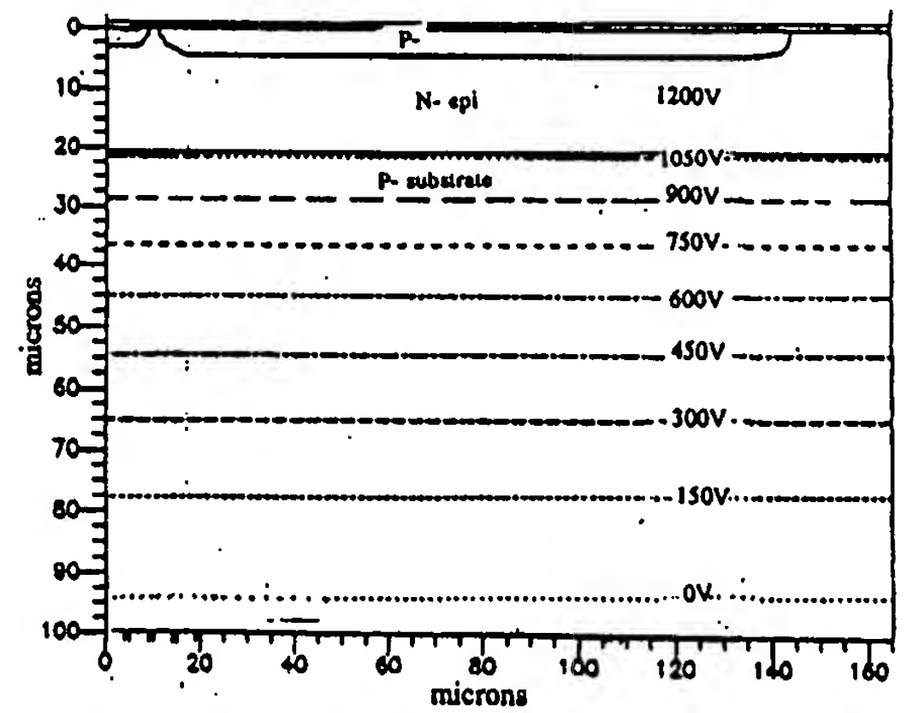

Fig. 5. Potential contours in the "two field-reduction layer" structure in the on-state (Drain and source at a hig potential relative to the grounded substrate) from PISCES simulations

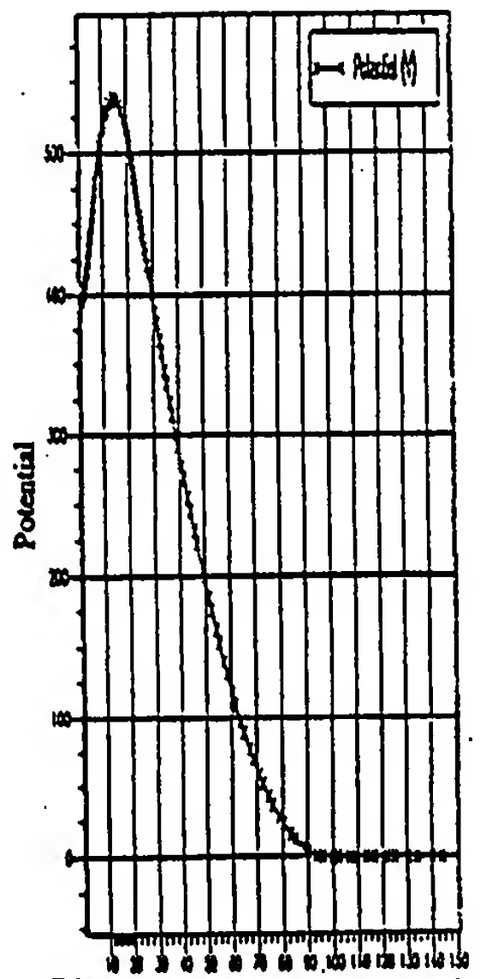

Fig. 6. Variation of potential through a vertical cross-section of the device at the center of the P- field-reduction region in the off-state from PISCES simulations

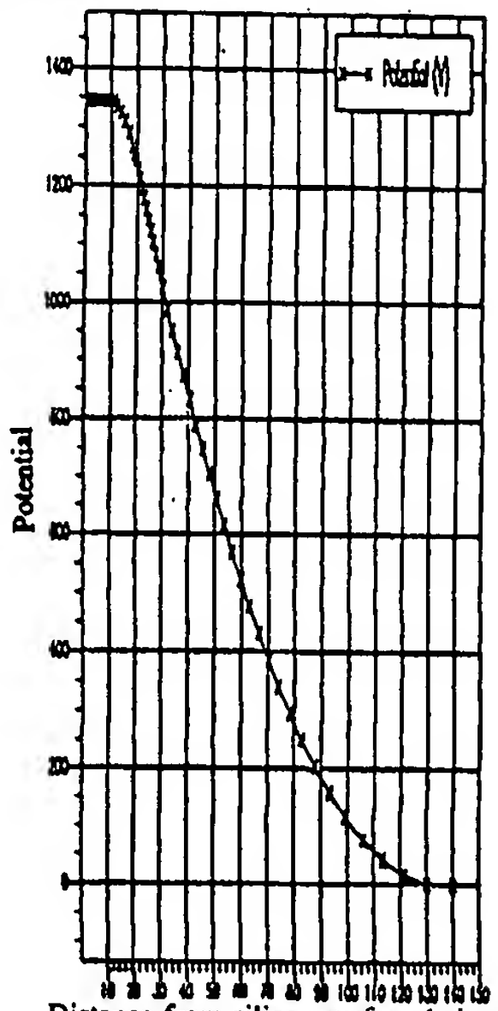

Fig. 7. Variation of potential through a vertical device section at the center of the P- field-reduction region in state from PISCES simulations

It can be seen from the potential distribution that in the off-state, the N- epi region is depleted from both the lower P-substrate/N- epi junction and the upper P- field-reduction layer/N- epi region. The on-state potential distribution shows that in the on-state, the N- epi is depleted only from the bottom P- substrate/N- epi junction leaving sufficient undepleted charge in the N- epi to allow low on-resistance on-state current conduction. Breakdown voltages in excess of 1200V were obtained from simulation of the off-state and on-state of the device structure in the high-side configuration.

Device Fabrication

The device was fabricated using International Rectifier High-Voltage Junction-Isolation (HVJI) Power IC Process which is summarized below:
The starting material used is a N- epi of resistivity in the range of 4 Ω-cm on a P- silicon substrate of resistivity in the range of 100 Ω-cm. The first step in the process is the growth of an oxide of approximately 1 μm. The first mask is used to define the P+ isolation regions and is followed by a long drive in at high temperature. After this, the second mask is used to define the P- field-reduction region. The P- field-reduction regions are implanted with boron with a total dose in the range of $4x10^{12}$ cm^{-2}.

This is followed by the growth of a field-oxide of thickness approximately 1 μm. The third mask is used to define deep-P+ regions under the N+ source regions of the MOSFET to increase its avalanche capability. The deep P+ regions are implanted with a boron dose of $4x10^{14}$ cm^{-2} after which drive in of deep-P+ is carried out. The next mask is used to define the active regions of the devices in the Power IC. A gate oxide of 825 Å is then grown after which Polysilicon is deposited. Mask 5 is used to define the Polysilicon gate regions. The P body and N+ source/drain regions of MOSFETs are defined next. This is followed by the contact mask to define the contact windows. Metal is then deposited and defined using Mask 9. This is followed by deposition of passivation layer followed by definition of the pad regions using Mask 10.

Experimental Results

The experimental results for the device structure shown in Fig 3 are summarized in Table 2 and in Fig 8-9 for two lots fabricated. High breakdown voltage is obtained by choosing the right combination of P- field-reduction layer implant dose, N- epi resistivity, P- substrate resistivity, P- field-reduction layer length and P- field-reduction layer/N+ drain spacing.

Table 2. Experimental results for the first lot of devices fabricated. The breakdown voltage (BV) of the devices was measured at a drain current of 10 μA. The on-resistance (R_{on}) was measured at a gate voltage of 10V with respect to the source and a drain current of 100 μA. The saturation current (I_{sat}) was measured at a gate voltage of 10V and a drain voltage of 10V with respect to the source.

SUBSTRATE RESISTIVITY (Ω-cm)	N- EPI RESISTIVITY (Ω-cm)	P- IMPLANT DOSE (cm^{-2})	P- LENGTH = 100 μm			P- LENGTH = 120 μm		
			BV (V)	R_{on} (Ω)	I_{sat} (mA)	BV (V)	R_{on} (Ω)	I_{sat} (mA)
40	4.12	$5.3x10^{12}$	680	760	29	860	820	29
100	4.07	$4.7x10^{12}$	880	690	37	970	750	37
100	5.16	$5.1x10^{12}$	900	685	37	1100	740	37
100	5.3	$4.1x10^{12}$	890	710	35	1000	780	35
100	4.73	$4.9x10^{12}$	1020	600	44	1100	650	43
100	4.78	$4.5x10^{12}$	1100	600	44	1100	650	44
100	4.7	$4.3x10^{12}$	1020	590	45	1150	640	44

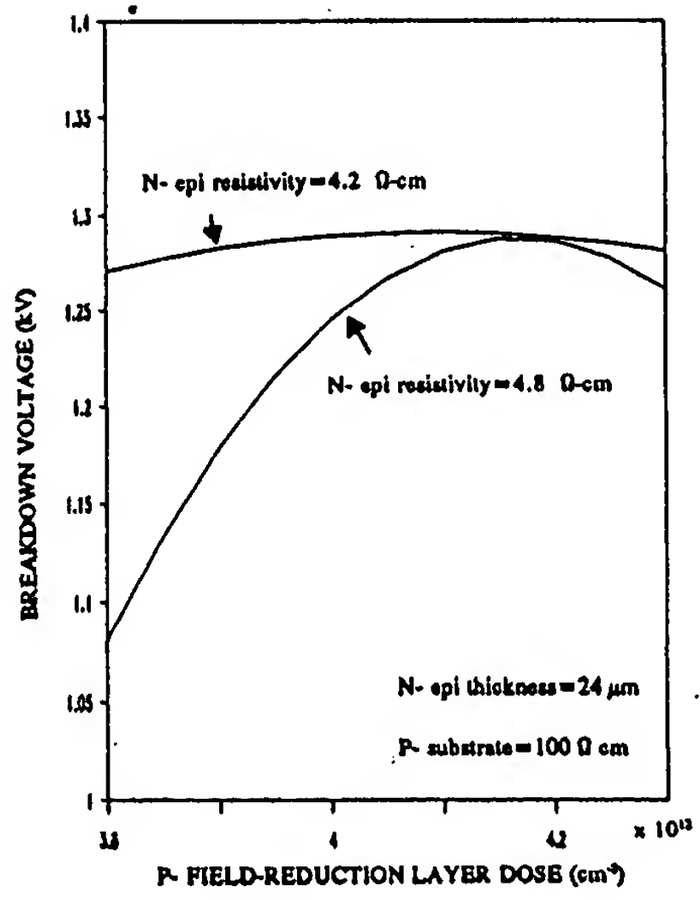

Fig. 8. Variation of breakdown voltage with P- field-reduction layer dose for the second lot of devices fabricated

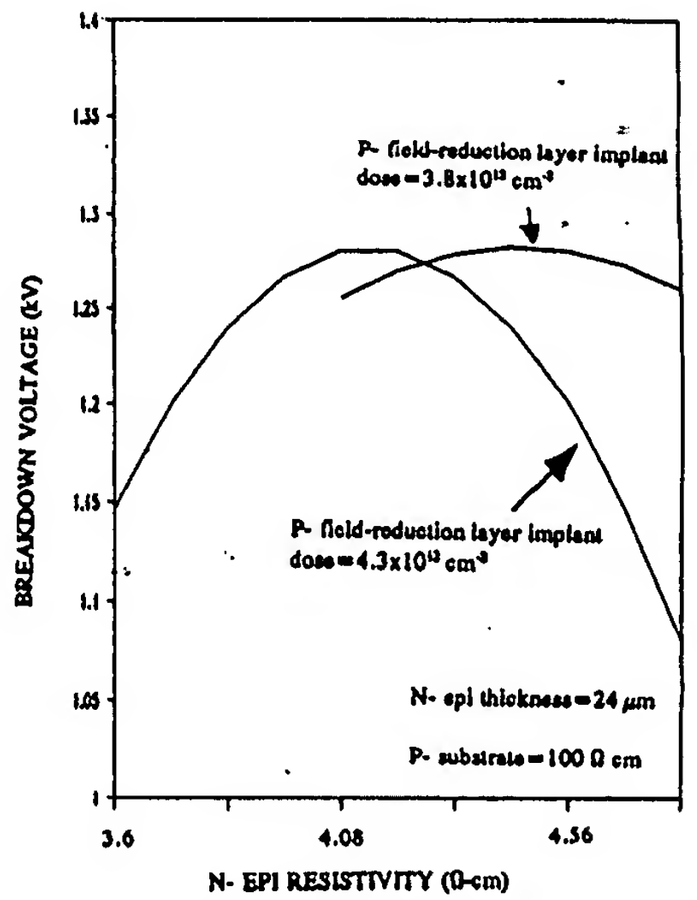

Fig. 9. Variation of breakdown voltage with N- resistivity for the second lot of devices fabricated

In our process, breakdown voltage close to 1300V was obtained by using a P- field-reduction layer implant dose of $4.1x10^{12}$ cm^{-2}, an N- epi resistivity of 4.2 Ω-cm and P-substrate resistivity of 100 Ω-cm. Another combination of parameters which resulted in breakdown voltage close to 1300V was a P- field-reduction layer implant dose of $3.8x10^{12}$ cm^{-2}, an N- epi resistivity of 4.5 Ω-cm and a 100 Ωcm P-substrate. The fabricated devices were of circular geometry with a P- field-reduction region length of 120 μm and had a on-resistance in the range of 900 Ω. The saturation current was in the range of 20 mA at a gate-to-source voltage of 10V. The devices were designed with a spacing of 15 μm between the P- field-reduction layer diffusion window and the N+ drain diffusion window.

Conclusions

The concept of using two field-reduction layers has b verified by two-dimensional device simulations and fabricating devices with breakdown voltage in excess 1200V using Junction-Isolated Power IC process. T concept is useful for lateral devices in high-side and low-s switching applications.

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[2] Dan Kinzer, "High power MOSFET and integr control circuit thereof for high-side sw application", US Patent 5023678, June 11, 1991

文献 2

Self-shielding: New High-Voltage Inter-Connection Technique for HVICs

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Abstract

A new, cost-effective, high-voltage inter-connection technique for HVICs, named SELF-SHIELDING, is proposed. To avoid the lowering of breakdown voltage of high-voltage devices affected by the electric potential of overlying inter-connections, self-shielding technique utilizes only the native PN-junction structures of high-voltage devices themselves. No additional shielding structure is required even to realize a very high-voltage IC above 1000V. Design concept and device structures are presented together with the experimental results on the operation of self-shielded 1200V level-shifters.

Introduction

The most critical theme for high-voltage integrated circuits (HVICs) is the electrical shielding of inter-connections from underlying high-voltage devices. If the inter-connections lying over high-voltage devices in HVIC are not properly shielded, the electric potential of inter-connections affect on the electric field distribution of underlying high-voltage devices. As a result, the breakdown voltage of the high-voltage devices are severely lowered.

To avoid this lowering of breakdown voltage, several approaches have been reported. Fixed potential shielding plates were successfully applied to 300-400V class HVICs [1,2]. Capacitively coupled field plates [3,4] and resistive field plate [5] obtained good results in 500-600V class HVICs. However, the extension of these techniques to higher voltage requires proportional increase of insulator thickness and additional conductive layers, to be resulted in the increase of cost and process difficulties. It was these limitations that prevented the development of HVIC far below 1000V.

In this paper, to breakthrough above mentioned limitations in conventional approaches, we propose a new shielding technique of high-voltage inter-connections for very high-voltage ICs; named SELF-SHIELDING [6]. After describing conventional HVIC, we demonstrate the design concept and device structures of self-shielded HVIC, followed by the experimental results on the operation of self-shielded, 1200V, n- and p-channel level-shifters.

0-7803-3106-0/96$5.00©1996 IEEE

Conventional HVIC

Typical block diagram and floor plan of conventional HVIC for driving totem-poled insulated-gate bipolar transistors (IGBTs) are shown in Fig. 1 (a) and Fig. 2 (a) , respectively. GDUH and GDUL in Fig. 1 are the driving circuits, respectively, for high- and low-side IGBTs. They are supplied driving power by low-voltage supplies (Vcc) connected to N terminal for GDUL and to O terminal for GDUH. Control unit in Fig. 1 is supplied by the same Vcc as GDUL and generates the timings for driving IGBTs, for example, to control a motor connected to O terminal. High-voltage main supply (Vdd) is connected between P and N terminals. As the potential of O terminal (Vo) swings between the potentials of P and N terminals (Vp and Vn) along with the switching of IGBTs, GDUH (Vo-level circuits) are isolated from GDUL and control unit (Vn-level circuits). To ensure this isolation, PN-junction-isolation and high-voltage junction termination (HVJT) techniques are used. For transmitting signals between Vo- and Vn-level circuits, level-shifters are provided utilizing high-voltage, n- and p-channel MOSFETs (HVN and HVP), load resistors, and voltage-clamping diodes.

In this design of conventional HVIC, high-voltage inter-connections (HV inter-connect.), H1 and H2, are crossing over HVJT respectively at two portions. At these portions, electric shielding is required to avoid the breakdown voltage lowering of HVJT affected by the electric potential of HV inter-connections. Conventional shielding techniques forced HVICs into increasing cost and process difficulties [1-5]. What is worse still, those process difficulties, mentioned earlier, limit the maximum breakdown voltage of conventional HVICs below 1000V.

Design Concept of Self-Shielding

In self-shielding concept, HV inter-connections do not cross over HVJT. Therefore, the electric potential of HV inter-connections are automatically shielded by self-junction structures of high-voltage devices.

Block diagram and floor plan of self-shielded HVIC are shown in Fig. 1 (b) and Fig. 2 (b), respectively. As seen from these figures, three loops of HVJT in conventional HVIC for

p⁻-substrate and the drain of HVP. The parasitic resistance causes undesirable leakage current parallel to the road resistors of level-shifters. As the parasitic resistance is unavoidable in proposed structures, it must be controlled to substantially high value for suppressing the power dissipation of self-shielded level-shifters.

Experimental Results

Experimental run has been performed to evaluate the applicability of self-shielding technique to very high-voltage ICs over 1000V. Substrates used were 230Ωcm, boron-doped, floating-zone-melted, silicon wafers and the process used was 3μm-CMOS. Evaluated devices were HVN, HVP, self-shielded HV n- and p-channel level-shifters, and the parasitic resistors of self-shielding regions. N- and p-channel level-shifters were laid into a single, complementary device. The photograph of a pair of complementary level-shifters is shown in Fig. 4.

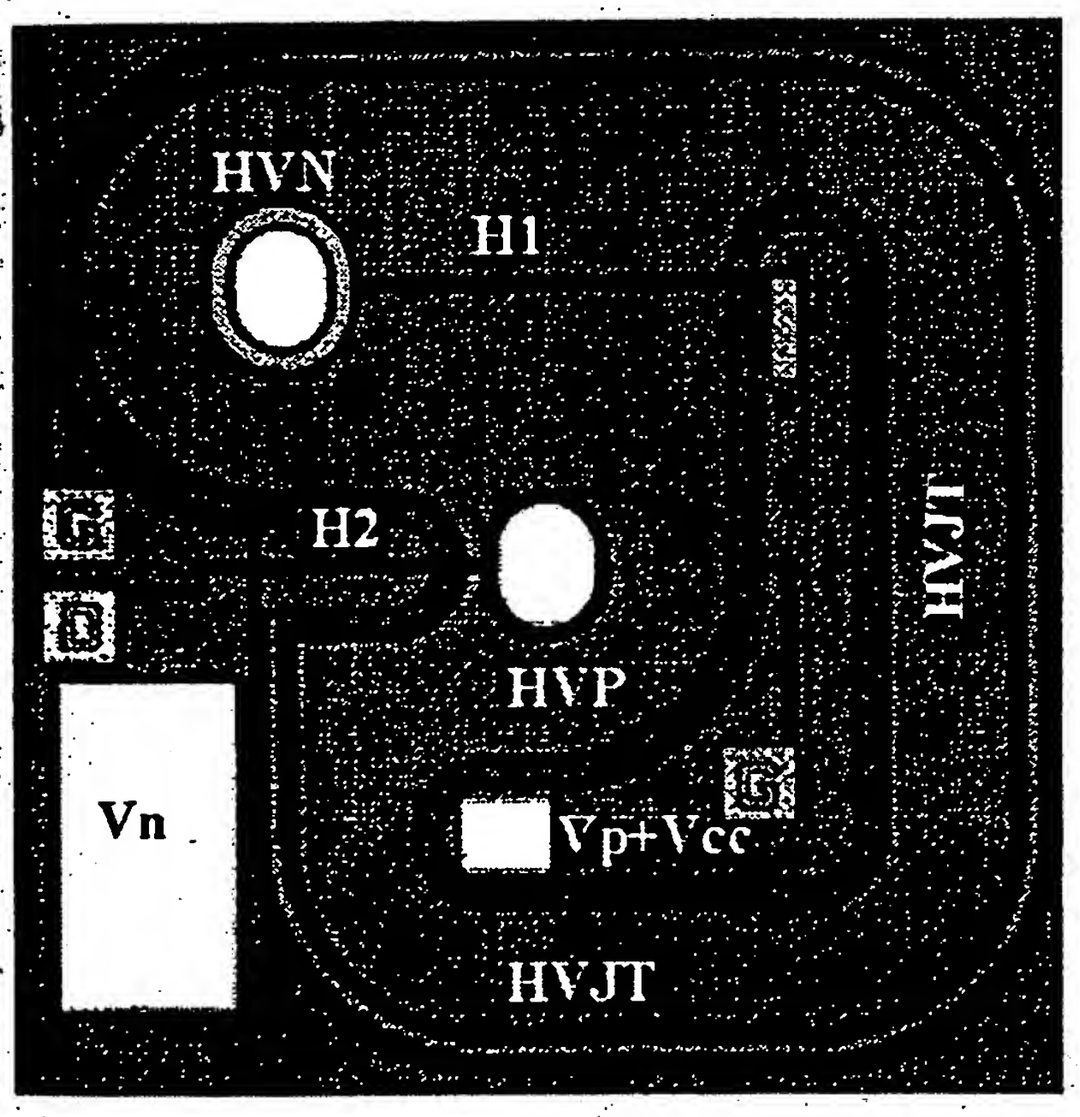
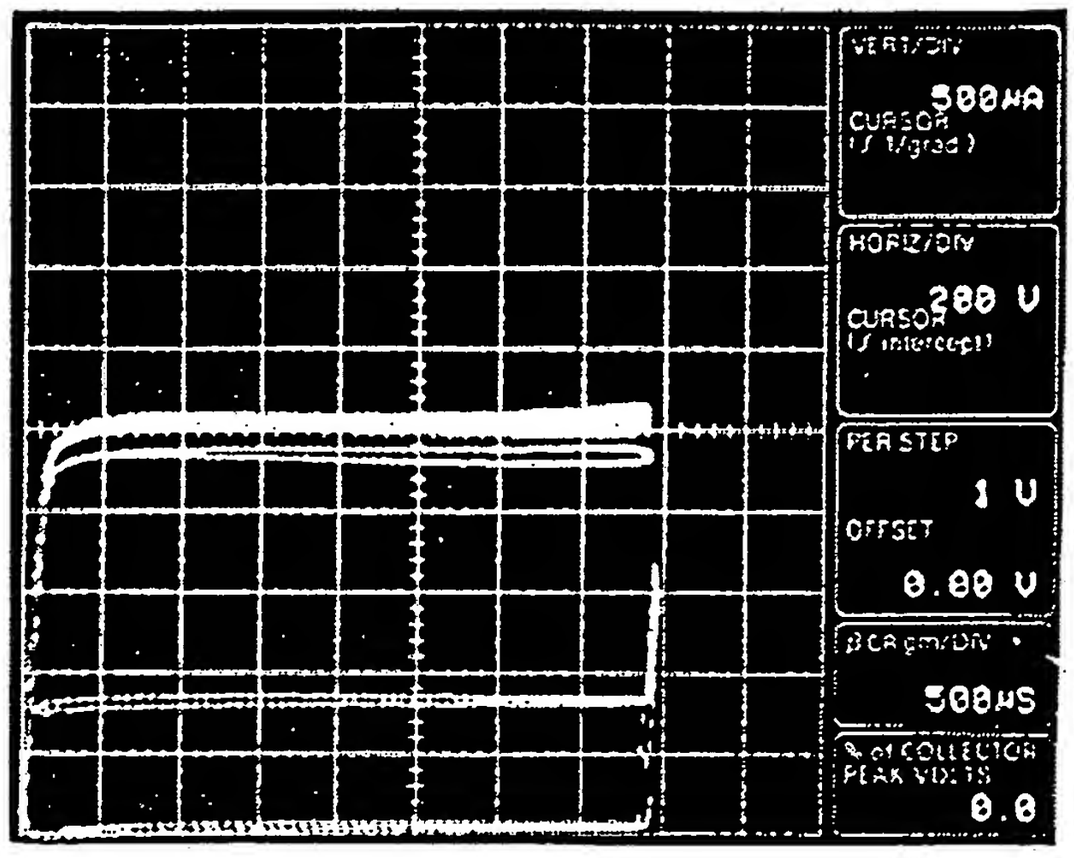
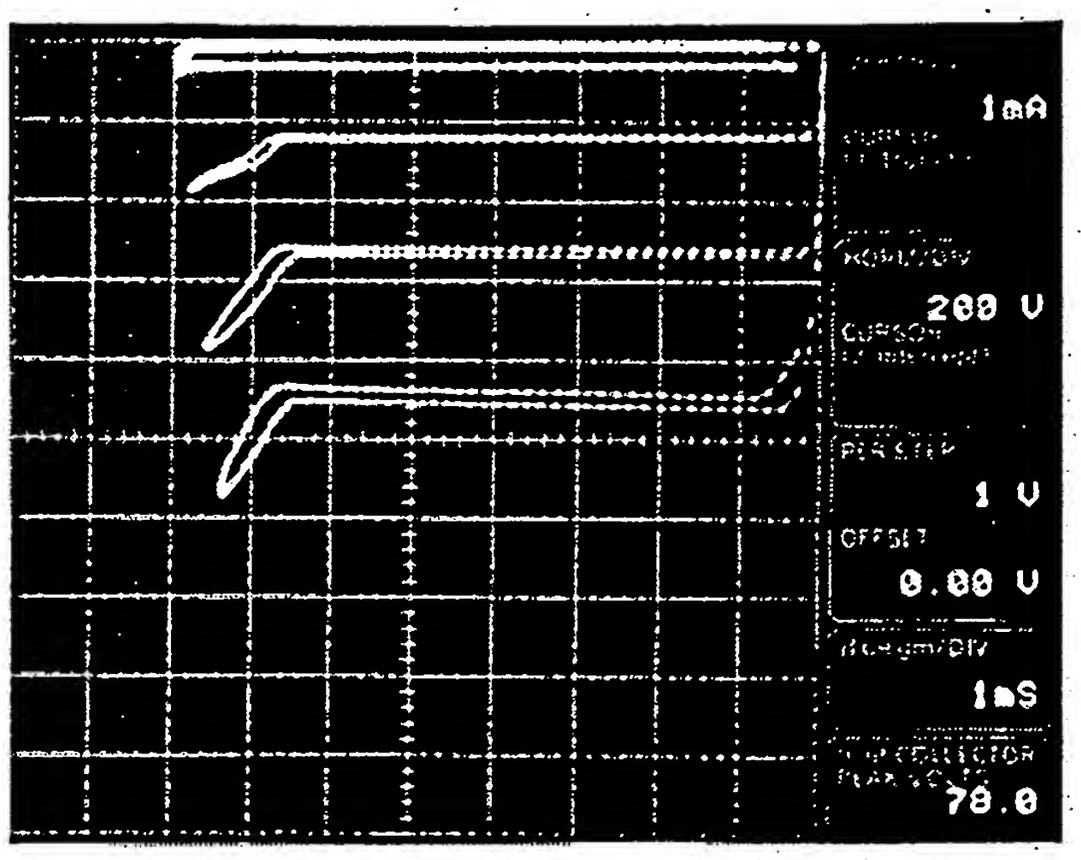


Fig. 4 Photograph of the experimental, complementary, self-shielded, high-voltage level-shifters in a single device layout.

The output characteristics of HVN and HVP are shown in Fig. 5 (a) and (b), respectively. Both HVN and HVP have a breakdown voltage of 1600V. As the doping of diffused regions were not optimized, the threshold voltage of HVN was much lower than that of HVP. The kink of output characteristics of HVP at high-current and high-voltage region is also due to the same reason. In HVN, the saturation of output current independent of gate voltage at higher gate



(a)



(b)

Fig. 5 Output characteristics of (a) HVN and (b) HVP.

voltage region comes from the effect of its double-base structure.

The operations of self-shielded, high-voltage, complementary level-shifters under 1200V supply are shown in Fig. 6 (a) and (b). The n-channel level-shifter converted the Vn-level, 0V/2V input signal to Vo-level, 1200V/1120V output signal. The p-channel level-shifter converted the Vo-level, 1200V/1185V input signal to Vn-level, 0V/40V signal. From these operation wave-forms, it is confirmed that the self-shielded level-shifters fulfill their function excellently in very high-voltage ICs.

For evaluating parasitic resistors, Rp1 and Rp2, leakage currents, Irp1 and Irp2, respectively through Rp1 and Rp2, were measured. They are plotted in Fig. 7 as a function of